NCP3170

Synchronous PWM Switching Converter

The NCP3170 is a flexible synchronous PWM Switching Buck Regulator. The NCP3170 operates from 4.5 V to 18 V, sourcing up to 3 A and is capable of producing output voltages as low as 0.8 V. The NCP3170 also incorporates current mode control. To reduce the number of external components, a number of features are internally set including soft start, power good detection, and switching frequency. The NCP3170 is currently available in an SOIC–8 package.

Features

- 4.5 V to 18 V Operating Input Voltage Range
- 90 mΩ High−Side, 25 mΩ Low−Side Switch
- FMEA Fault Tolerant During Pin Short Test
- 3 A Continuous Output Current
- Fixed 500 kHz and 1 MHz PWM Operation
- Cycle−by−Cycle Current Monitoring
- 1.5% Initial Output Accuracy
- Internal 4.6 ms Soft−Start
- Short−Circuit Protection
- Turn on Into Pre−bias
- Power Good Indication
- Light Load Efficiency
- Thermal Shutdown
- These are Pb−Free Devices

Typical Applications

- Set Top Boxes
- DVD/ Blu−ray™ Drives and HDD
- LCD Monitors and TVs
- Cable Modems
- PCIe Graphics Cards
- Telecom/Networking/Datacom Equipment
- Point of Load DC/DC Converters

Figure 1. Typical Application Circuit
NCP3170

Figure 2. NCP3170 Block Diagram

### PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PGND</td>
<td>The power ground pin is the high current path for the device. The pin should be soldered to a large copper area to reduce thermal resistance. PGND needs to be electrically connected to AGND.</td>
</tr>
<tr>
<td>2</td>
<td>VIN</td>
<td>The input voltage pin powers the internal control circuitry and is monitored by multiple voltage comparators. The VIN pin is also connected to the internal power PMOS switch and linear regulator output. The VIN pin has high di/dt edges and must be decoupled to ground close to the pin of the device.</td>
</tr>
<tr>
<td>3</td>
<td>AGND</td>
<td>The analog ground pin serves as small-signal ground. All small-signal ground paths should connect to the AGND pin and should also be electrically connected to power ground at a single point, avoiding any high current ground returns.</td>
</tr>
<tr>
<td>4</td>
<td>FB</td>
<td>Inverting input to the OTA error amplifier. The FB pin in conjunction with the external compensation serves to stabilize and achieve the desired output voltage with current mode compensation.</td>
</tr>
<tr>
<td>5</td>
<td>COMP</td>
<td>The loop compensation pin is used to compensate the transconductance amplifier which stabilizes the operation of the converter stage. Place compensation components as close to the converter as possible. Connect a RC network between COMP and AGND to compensate the control loop.</td>
</tr>
<tr>
<td>6</td>
<td>EN</td>
<td>Enable pin. Pull EN to logic high to enable the device. Pull EN to logic low to disable the device. Do not leave it open.</td>
</tr>
<tr>
<td>7</td>
<td>PG</td>
<td>Power good is an open drain 500 μA pull down indicating output voltage is within the power good window. If the power good function is not used, it can be connected to the VSW node to reduce thermal resistance. Do not connect PG to the VSW node if the application is turning on into pre-bias.</td>
</tr>
<tr>
<td>8</td>
<td>VSW</td>
<td>The VSW pin is the connection of the drains of the internal N and P MOSFETs. At switch off, the inductor will drive this pin below ground as the body diode and the NMOS conducts with a high dv/dt.</td>
</tr>
</tbody>
</table>
ABSOLUTE MAXIMUM RATINGS (measured vs. GND pin 3, unless otherwise noted)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>( V_{\text{MAX}} )</th>
<th>( V_{\text{MIN}} )</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Supply Voltage Input</td>
<td>( V_{\text{IN}} )</td>
<td>20</td>
<td>(-0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Voltage between PGND and AGND</td>
<td>( V_{\text{PAG}} )</td>
<td>0.3</td>
<td>(-0.3)</td>
<td>V</td>
</tr>
<tr>
<td>PWM Feedback Voltage</td>
<td>( F_{\text{B}} )</td>
<td>6</td>
<td>(-0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Error Amplifier Voltage</td>
<td>( \text{COMP} )</td>
<td>6</td>
<td>(-0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Enable Voltage</td>
<td>( \text{EN} )</td>
<td>( V_{\text{IN}} + 0.3 ) V</td>
<td>(-0.3)</td>
<td>V</td>
</tr>
<tr>
<td>PG Voltage</td>
<td>( \text{PG} )</td>
<td>( V_{\text{IN}} + 0.3 ) V</td>
<td>(-0.3)</td>
<td>V</td>
</tr>
<tr>
<td>VSW to AGND or PGND</td>
<td>( V_{\text{SW}} )</td>
<td>( V_{\text{IN}} + 0.3 ) V</td>
<td>(-0.7)</td>
<td>V</td>
</tr>
<tr>
<td>VSW to AGND or PGND for 35ns</td>
<td>( V_{\text{SWST}} )</td>
<td>( V_{\text{IN}} + 10 ) V</td>
<td>(-5)</td>
<td>V</td>
</tr>
<tr>
<td>Junction Temperature (Note 1)</td>
<td>( T_{\text{J}} )</td>
<td>+150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>( T_{\text{A}} )</td>
<td>(-40) to +85</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>( T_{\text{stg}} )</td>
<td>(-55) to +150</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

Thermal Characteristics (Note 2)

| SOIC–8 Plastic Package                              | |
| Maximum Power Dissipation @ \( T_{\text{A}} = 25^\circ\text{C} \) | \( P_{\text{D}} \) | 1.15 | W |
| Thermal Resistance Junction–to–Air                 | \( R_{\text{JA}} \) | 87  | °C/W |
| Thermal Resistance Junction–to–Case                | \( R_{\text{JC}} \) | 37.8 | °C/W |
| Lead Temperature Soldering (10 sec):                | \( RF \) | 260 peak | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The maximum package power dissipation limit must not be exceeded.
   \[
   P_{\text{D}} = \frac{T_{\text{J(max)}} - T_{\text{A}}}{R_{\text{JA}}}
   \]

2. The value of \( R_{\text{JA}} \) is measured with the device mounted on a 2in x 2in FR–4 board with 2oz. copper, in a still air environment with \( T_{\text{A}} = 25^\circ\text{C} \).
   The value in any given application depends on the user’s specific board design.

3. 60–180 seconds minimum above 237°C.

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Supply Voltage Input</td>
<td>( V_{\text{IN}} )</td>
<td>4.5</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>Power Good Pin Voltage</td>
<td>( PG )</td>
<td>4.5</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>Switch Pin Voltage</td>
<td>( V_{\text{SW}} )</td>
<td>(-0.3)</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>Enable Pin Voltage</td>
<td>( \text{EN} )</td>
<td>0</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>Comp Pin Voltage</td>
<td>( \text{COMP} )</td>
<td>(-0.1)</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Feedback Pin Voltage</td>
<td>( \text{FB} )</td>
<td>(-0.1)</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Power Ground Pin Voltage</td>
<td>( \text{PGND} )</td>
<td>(-0.1)</td>
<td>(-0.1)</td>
<td>V</td>
</tr>
<tr>
<td>Junction Temperature Range</td>
<td>( T_{\text{J}} )</td>
<td>(-40)</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>( T_{\text{A}} )</td>
<td>(-40)</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>
### NCP3170

**ELECTRICAL CHARACTERISTICS** (\(T_A = 25\,^\circ\text{C}, \, V_{IN} = V_{EN} = 12\, \text{V}, \, V_{OUT} = 3.3\, \text{V}\) for min/max values unless otherwise noted (Note 7))

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>(Note 5)</td>
<td>4.5</td>
<td>18</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**SUPPLY CURRENT**

<p>| | | | | | |</p>
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<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Quiescent Supply Current</td>
<td>NCP3170A, NCP3170B</td>
<td>1.7</td>
<td>1.7</td>
<td>2.0</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>(V_{IN} = EN = 12, \text{V}, V_{FB} = 0.8, \text{V}) (Note 5)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown Supply Current</td>
<td>EN = 0 \text{V} (Note 5)</td>
<td>13</td>
<td>17</td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
</tbody>
</table>

**UNDER VOLTAGE LOCKOUT**

<p>| | | | | | |</p>
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</tr>
</thead>
<tbody>
<tr>
<td>VIN UVLO Threshold</td>
<td>(V_{IN}) Rising Edge (Note 5)</td>
<td>4.41</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIN UVLO Threshold</td>
<td>(V_{IN}) Falling Edge (Note 5)</td>
<td>4.13</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**MODULATOR**

<p>| | | | | | |</p>
<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Oscillator Frequency</td>
<td>NCP3170A, NCP3170B</td>
<td>450</td>
<td>900</td>
<td>500</td>
<td>1100</td>
</tr>
<tr>
<td></td>
<td>Enable = (V_{IN})</td>
<td>900</td>
<td>1800</td>
<td>1100</td>
<td>2300</td>
</tr>
<tr>
<td>Maximum Duty Ratio</td>
<td>NCP3170A, NCP3170B</td>
<td>91</td>
<td>90</td>
<td>96</td>
<td>96</td>
</tr>
<tr>
<td>Minimum Duty Ratio</td>
<td>NCP3170A, NCP3170B</td>
<td>6.0</td>
<td>4.0</td>
<td>11.5</td>
<td>11.5</td>
</tr>
<tr>
<td>VIN Soft Start Ramp Time</td>
<td>(V_{FB} = V_{COMP})</td>
<td>3.5</td>
<td>4.6</td>
<td>6.0</td>
<td>ms</td>
</tr>
</tbody>
</table>

**OVER CURRENT**

<p>| | | | | | |</p>
<table>
<thead>
<tr>
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<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Limit</td>
<td>(Note 4)</td>
<td>4.0</td>
<td>6.0</td>
<td>A</td>
<td></td>
</tr>
</tbody>
</table>

**PWM COMPENSATION**

<p>| | | | | | |</p>
<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>VFB Feedback Voltage</td>
<td>(T_A = 25,^\circ\text{C})</td>
<td>0.792</td>
<td>0.8</td>
<td>0.808</td>
<td>V</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>(Note 4)</td>
<td>1</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>GM</td>
<td>(Note 4)</td>
<td>201</td>
<td></td>
<td></td>
<td>(\mu\text{S})</td>
</tr>
<tr>
<td>A0 DC gain</td>
<td>(Note 4)</td>
<td>40</td>
<td>55</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Unity Gain BW ((C_{OUT} = 10, \text{pF}))</td>
<td>(Note 4)</td>
<td>2.0</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>(Current Out of FB IB Pin)</td>
<td>286</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>IEAOP Output Source Current</td>
<td>(V_{FB} = 0, \text{V})</td>
<td>20.1</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>IEAOM Output Sink Current</td>
<td>(V_{FB} = 2, \text{V})</td>
<td>21.3</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
</tbody>
</table>

**ENABLE**

<p>| | | | | | |</p>
<table>
<thead>
<tr>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable Threshold</td>
<td>(Note 5)</td>
<td>1.41</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**POWER GOOD**

<p>| | | | | | |</p>
<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Power Good High On Threshold</td>
<td></td>
<td>875</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Power Good High Off Threshold</td>
<td></td>
<td>859</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Power Good Low On Threshold</td>
<td></td>
<td>712</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Power Good Low Off Threshold</td>
<td></td>
<td>728</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Over Voltage Protection Threshold</td>
<td></td>
<td>998</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Power Good Low Voltage</td>
<td>(V_{IN} = 12, \text{V}, IPG = 500, \mu\text{A})</td>
<td>0.195</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**PWM OUTPUT STAGE**

<p>| | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>High–Side Switch On–Resistance</td>
<td>(V_{IN} = 12, \text{V}) (V_{IN} = 4.5, \text{V})</td>
<td>90</td>
<td>130</td>
<td>150</td>
<td>m\Omega</td>
</tr>
<tr>
<td>Low–Side Switch On–Resistance</td>
<td>(V_{IN} = 12, \text{V}) (V_{IN} = 4.5, \text{V})</td>
<td>25</td>
<td>35</td>
<td>39</td>
<td>m\Omega</td>
</tr>
</tbody>
</table>

**THERMAL SHUTDOWN**

<p>| | | | | | |</p>
<table>
<thead>
<tr>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Shutdown</td>
<td>(Notes 4 and 6)</td>
<td>164</td>
<td></td>
<td></td>
<td>(^\circ\text{C})</td>
</tr>
<tr>
<td>Hysteresis</td>
<td></td>
<td>43</td>
<td></td>
<td></td>
<td>(^\circ\text{C})</td>
</tr>
</tbody>
</table>

4. Guaranteed by design
5. Ambient temperature range of \(-40\,^\circ\text{C}\) to \(+85\,^\circ\text{C}\).
6. This is not a protection feature.
7. The device is not guaranteed to operate beyond the maximum operating ratings.
TYPICAL PERFORMANCE CHARACTERISTICS
(Circuit from Figure 1, TA = 25°C, VIN = VEN = 12 V, VOUT = 3.3 V unless otherwise specified)

Figure 3. Light Load (DCM) Operation 1 μs/DIV

Figure 4. Full Load (CCM) Operation 1 μs/DIV

Figure 5. Start-Up into Full Load 1 ms/DIV

Figure 6. Short-Circuit Protection 200 μs /DIV

Figure 7. 50% to 100% Load Transient 100 μs/DIV

Figure 8. 3.3 V Turn on into 1 V Pre-Bias 1 ms /DIV
TYPICAL PERFORMANCE CHARACTERISTICS
(Circuit from Figure 1, TA = 25°C, VIN = VEN = 12 V, VOUT = 3.3 V unless otherwise specified)

Figure 9. ICC Shut Down Current vs. Temperature

Figure 10. NCP3170 Enabled Current vs. Temperature

Figure 11. Bandgap Reference Voltage vs. Temperature

Figure 12. Switching Frequency vs. Temperature

Figure 13. Input Under Voltage Protection at 12 V vs. Temperature

Figure 14. Input Over Voltage Protection at 12 V vs. Temperature
NCP3170

TYPICAL PERFORMANCE CHARACTERISTICS
(Circuit from Figure 1, TA = 25°C, VIN = VEN = 12 V, VOUT = 3.3 V unless otherwise specified)

Figure 15. High Side MOSFET $R_{DS(on)}$ vs. Temperature

Figure 16. Low Side MOSFET $R_{DS(on)}$ vs. Temperature

Figure 17. Transconductance vs. Temperature

Figure 18. Over Voltage Protection vs. Temperature

Figure 19. Input Under Voltage Protection vs. Temperature
NCP3170A Efficiency and Thermal Derating

Thermal derating curves for the SOIC−8 package part under typical input and output conditions based on the evaluation board. The ambient temperature is 25°C with natural convection (air speed < 50 LFM) unless otherwise specified.
NCP3170

NCP3170B Efficiency and Thermal Derating

Thermal derating curves for the SOIC–8 package part under typical input and output conditions based on the evaluation board. The ambient temperature is 25°C with natural convection (air speed < 50 LFM) unless otherwise specified.
The NCP3170 is a current-mode, step down regulator with an integrated high-side PMOS switch and a low-side NMOS switch. It operates from a 4.5 V to 18 V input voltage range and supplies up to 3 A of load current. The duty ratio can be adjusted from 8% to 92% allowing a wide output voltage range. Features include enable control, Power-On Reset (POR), input under voltage lockout, fixed internal soft start, power good indication, over voltage protection, and thermal shutdown.

**Enable and Soft-Start**

An internal input voltage comparator not shown in Figure 28 will force the part to disable below the minimum input voltage of 4.13 V. The input under voltage disable feature is used to prevent improper operation of the converter due to insufficient voltages. The converter can be turned on by tying the enable pin high and the part will default to be input voltage enabled. The enable pin should never be left floating.

If an adjustable Under Voltage Lockout (UVLO) threshold is required, the EN pin can be used. The trip voltage of the EN pin comparator is 1.38 V typical. Upon application of an input voltage greater than 4.41 V, the VIN UVLO will release and the enable will be checked to determine if switching can commence. Once the 1.38 V trip voltage is crossed, the part will enable and the soft start sequence will initiate. If large resistor values are used, the EN pin should be bypassed with a 1 nF capacitor to prevent coupling problems from the switch node.

The enable pin can be used to delay a turn on by connecting a capacitor as shown in Figure 30.

If the designer would like to add hysteresis to the enable threshold it can be added by use of a bias resistor to the output. The hysteresis is created once soft start has initiated. With the output voltage rising, current flows into the enable node, raising the voltage. The thresholds for enable as well as hysteresis can be calculated using Equation 1.

\[
\text{VIN}_{\text{HYS}} = \text{VIN}_{\text{Start}} - \text{EN}_{\text{TH}} + R_{1_{\text{UV}}}
\times \left[ \frac{V_{\text{OUT}} - \text{EN}_{\text{TH}}}{R_{3_{\text{UV}}}} - \frac{\text{EN}_{\text{TH}}}{R_{2_{\text{UV}}}} \right] \quad \text{(eq. 1)}
\]

\[
\text{VIN}_{\text{Start}} = \text{EN}_{\text{TH}} \times \left[ 1 + \frac{R_{1_{\text{UV}}} \times (R_{2_{\text{UV}}} + R_{3_{\text{UV}}})}{R_{2_{\text{UV}}} \times R_{3_{\text{UV}}}} \right]
\]

**Definitions:**

- \( \text{EN}_{\text{TH}} \) = Enable Threshold
- \( \text{VIN}_{\text{START}} \) = Input Voltage Start Threshold
- \( R_{1_{\text{UV}}} \) = High Side Resistor
- \( R_{2_{\text{UV}}} \) = Low Side Resistor
- \( R_{3_{\text{UV}}} \) = Hysteresis Bias Resistor
- \( V_{\text{OUT}} \) = Regulated Output Voltage
The part can be enabled with standard TTL or high voltage logic by using the configuration below.

![Figure 32. Logic Turn–on](image)

The enable can also be used for power sequencing in conjunction with the Power Good (PG) pin as shown in Figure 33. The enable pin can either be tied to the output voltage of the master voltage or tied to the input voltage with a resistor to the PG pin of the master regulator.

![Figure 33. Enable Two Converter Power Sequencing](image)

Once the part is enabled, the internal reference voltage is slewed from ground to the set point of 800 mV. The slewing process occurs over a 4.5 ms period, reducing the current draw from the upstream power source, reducing stress on internal MOSFETS, and ensuring the output inductor does not saturate during start-up.

**Pre–Bias Start–up**

When starting into a pre–bias load, the NCP3170 will not discharge the output capacitors. The soft start begins with the internal reference at ground. Both the high side switch and low side switches are turned off. The internal reference slowly raises and the OTA regulates the output voltage to the divided reference voltage. In a pre–biased condition, the voltage at the FB pin is higher than the internal reference voltage, so the OTA will keep the COMP voltage at ground potential. As the internal reference is slewed up, the COMP pin is held low until the FB pin voltage surpasses the internal reference voltage, at which time the COMP pin is allowed to respond to the OTA error signal. Since the bottom of the PWM ramp is at 0.6 V there will be a slight delay between the time the internal reference voltage passes the FB voltage and when the part starts to switch. Once the COMP error signal intersects with the bottom of the ramp, the high side switch is turned on followed by the low side switch. After the internal reference voltage has surpassed the FB voltage, soft start proceeds normally without output voltage discharge.

**Power Good**

The output voltage of the buck converter is monitored at the feedback pin of the output power stage. Two comparators are placed on the feedback node of the OTA to monitor the operating window of the feedback voltage as shown in Figure 34. All comparator outputs are ignored during the soft start sequence as soft start is regulated by the OTA since false trips would be generated. Further, the PG pin is held low until the comparators are evaluated. PG state does not affect the switching of the converter. After the soft start period has ended, if the feedback is below the reference voltage of comparator 1 ($V_{FB} < 0.726$), the output is considered operational undervoltage (OUV). The device will indicate the under voltage situation by the PG pin remaining low with a 100 kΩ pull–up resistance. When the feedback pin voltage rises between the reference voltages of comparator 1 and comparator 2 ($0.726 < V_{FB} < 0.862$), then the output voltage is considered power good and the PG pin is released. Finally, if the feedback voltage is greater than comparator 2 ($V_{FB} > 0.862$), the output voltage is considered operational overvoltage (OOV). The OOV will be indicated by the PG pin remaining low. A block diagram of the OOV and OUV functionality as well as a graphical representation of the PG pin functionality is shown in Figures 34 through 36.

![Figure 34. OOV and OUV System](image)

![Figure 35. OOV and OUV Window](image)
If the power good function is not used, it can be connected to the VSW node to reduce thermal resistance. Do not connect PG to the VSW node if the application is turning on into pre–bias.

Switching Frequency

The NCP3170 switching frequency is fixed and set by an internal oscillator. The practical switching frequency could range from 450 kHz to 550 kHz for the NCP3170A and 900 kHz to 1.1 MHz for the NCP3170B due to device variation.

Light Load Operation

Light load operation is generally a load that is 1mA to 300 mA where a load is in standby mode and requires very little power. During light load operation, the regulator emulates the operation of a non–synchronous buck converter and the regulator is allowed to skip pulses. The non–synchronous buck emulation is accomplished by detecting the point at which the current flowing in the inductor goes to zero and turning the low side switch off. At the point when the current goes to zero, if the low side switch is not turned off, current would reverse, discharging the output capacitor. Since the low side switch is shutoff, the only conduction path is through the body diode of the low side MOSFET, which is back biased. Unlike traditional synchronous buck converters, the current in the inductor will become discontinuous. As a result, the switch node will oscillate with the parasitic inductances and capacitances connected to the switch node. The OTA will continue to regulate the output voltage, but will skip pulses based on the output load shown in Figure 37.

Protection Features

Over Current Protection

Current is limited to the load on a pulse by pulse basis. During each high side on period, the current is compared against an internally set limit. If the current limit is exceeded the high side and low side MOSFEts are shutoff and no pulses are issued for 13.5 μs. During that time, the output voltage will decay and the inductor current will discharge. After the discharge period, the converter will initiate a soft start. If the load is not released, the current will build in the inductor until the current limit is exceeded, at which time the high side and low side MOSFETs will be shut off and the process will continue. If the load has been released, a normal soft start will commence and the part will continue switching normally until the current limit is exceeded.

Thermal Shutdown

The thermal limit, while not a protection feature, engages at 150°C in case of thermal runaway. When the thermal comparator is tripped at a die temperature of 150°C, the part must cool to 120°C before a restart is allowed. When thermal trip is engaged, switching ceases and high side and low side MOSFETs are driven off. Further, the power good indicator will pull low until the thermal trip has been released. Once the die temperature reaches 120°C the part will reinitiate soft–start and begin normal operation.
Over Voltage Protection

Upon the completion of soft start, the output voltage of the buck converter is monitored at the FB pin of the output power stage. One comparator is placed on the feedback node to provide over voltage protection. In the event an over voltage is detected, the high side switch turns off and the low side switch turns on until the feedback voltage falls below the OOV threshold. Once the voltage has fallen below the OOV threshold, switching continues normally as displayed in Figure 40.

Duty Ratio

The duty ratio can be adjusted from 8% to 92% allowing a wide output voltage range. The low 8% duty ratio limit will restrict the PWM operation. For example if the application is converting to 1.2 V the converter will perform normally if the input voltage is below 15.5 V. If the input voltage exceeds 15.5 V while supplying 1.2 V output voltage the converter can skip pulses during operation. The skipping pulse operation will result in higher ripple voltage than when operating in PWM mode. Figure 41 and 42 below shows the safe operating area for the NCP3170A and B respectively. While not shown in the safe operating area graph, the output voltage is capable of increasing to the 93% duty ratio limitation providing a high output voltage such as 16 V. If the application requires a high duty ratio such as converting from 14 V to 10 V the converter will operate normally until the maximum duty ratio is reached. For example, if the input voltage were 16 V and the user wanted to produce the highest possible output voltage at full load, a good rule of thumb is to use 80% duty ratio. The discrepancy between the usable duty ratio and the actual duty ratio is due to the voltage drops in the system, thus leading to a maximum output voltage of 12.8 V rather than 14.8 V. The actual achievable output to input voltage ratio is dependent on layout, component selection, and acceptable output voltage tolerance.

Design Procedure

When starting the design of a buck regulator, it is important to collect as much information as possible about the behavior of the input and output before starting the design. ON Semiconductor has a Microsoft Excel® based design tool available online under the design tools section of the NCP3170 product page. The tool allows you to capture your design point and optimize the performance of your regulator based on your design criteria.

<table>
<thead>
<tr>
<th>Design Parameter</th>
<th>Example Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (V\text{IN})</td>
<td>9 V to 16 V</td>
</tr>
<tr>
<td>Output Voltage (V\text{OUT})</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Input Ripple Voltage (V\text{Cripple})</td>
<td>200 mV</td>
</tr>
<tr>
<td>Output Ripple Voltage (V\text{OUTripples})</td>
<td>20 mV</td>
</tr>
<tr>
<td>Output Current Rating (I\text{OUT})</td>
<td>3 A</td>
</tr>
<tr>
<td>Operating Frequency (F\text{SW})</td>
<td>500 kHz</td>
</tr>
</tbody>
</table>
The buck converter produces input voltage ($V_{IN}$) pulses that are LC filtered to produce a lower DC output voltage ($V_{OUT}$). The output voltage can be changed by modifying the on time relative to the switching period ($T$) or switching frequency. The ratio of high side switch on time to the switching period is called duty ratio ($D$). Duty ratio can also be calculated using $V_{OUT}$, $V_{IN}$, the Low Side Switch Voltage Drop ($V_{LSD}$), and the High Side Switch Voltage Drop ($V_{HSD}$).

$$D = \frac{TON}{T} \times (1 - D) \rightarrow \frac{T_{OFF}}{T}$$

$$D = \frac{V_{OUT} + V_{LSD}}{V_{IN} - V_{HSD} + V_{LSD}}$$

$$D = \frac{V_{OUT}}{V_{IN}} \rightarrow 27.5\% = \frac{3.3 \text{ V}}{12 \text{ V}}$$

$D$ = Duty ratio
$FSW$ = Switching frequency
$T$ = Switching period
$TOFF$ = High side switch off time
$TON$ = High side switch on time
$V_{IN}$ = Input voltage
$V_{HSD}$ = High side switch voltage drop
$V_{LSD}$ = Low side switch voltage drop
$V_{OUT}$ = Output voltage

### Inductor Selection

When selecting an inductor, the designer may employ a rule of thumb for the design where the percentage of ripple current in the inductor should be between 10% and 40%. When using ceramic output capacitors, the ripple current can be greater because the ESR of the output capacitor is smaller, thus a user might select a higher ripple current. However, when using electrolytic capacitors, a lower ripple current will result in lower output ripple due to the higher ESR of electrolytic capacitors. The ratio of ripple current to maximum output current is given in Equation 5.

$$ra = \frac{\Delta I}{I_{OUT}}$$

$\Delta I$ = Ripple current
$I_{OUT}$ = Output current
$ra$ = Ripple current ratio

Using the ripple current rule of thumb, the user can establish acceptable values of inductance for a design using Equation 6.

$$L_{OUT} = \frac{V_{OUT}}{I_{OUT} \times ra \times F_{SW}} \times (1 - D) \rightarrow$$

$$4.7 \mu\text{H} = \frac{12 \text{ V}}{3.0 \text{ A} \times 34\% \times 500 \text{ kHz}} \times (1 - 27.5\%)$$

When selecting an inductor, the designer must not exceed the current rating of the part. To keep within the bounds of the part’s maximum rating, a calculation of the RMS current and peak current are required.

$$I_{RMS} = I_{OUT} \times \sqrt{1 + \frac{ra^2}{12}} \rightarrow$$

$$3.01 \text{ A} = 3 \text{ A} \times \sqrt{1 + \frac{34\%^2}{12}}$$

$$I_{OUT} = \text{Output current}$$
$$I_{RMS} = \text{Inductor RMS current}$$
$$ra = \text{Ripple current ratio}$$

$$I_{PK} = I_{OUT} \times \left(1 + \frac{ra}{2}\right) \rightarrow$$

$$3.51 \text{ A} = 3 \text{ A} \times \left(1 + \frac{34\%}{2}\right)$$

$I_{OUT}$ = Output current
$I_{PK}$ = Inductor peak current
$ra$ = Ripple current ratio
A standard inductor should be found so the inductor will be rounded to 4.7 μH. The inductor should support an RMS current of 3.01 A and a peak current of 3.51 A. A good design practice is to select an inductor that has a saturation current that exceeds the maximum current limit with some margin.

The final selection of an output inductor has both mechanical and electrical considerations. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the regulation system, a minimum inductor value is particularly important in space constrained applications. From an electrical perspective, the maximum current slew rate through the output inductor for a buck regulator is given by Equation 9.

\[
\text{SlewRate}_{\text{OUT}} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{L_{\text{OUT}}} \quad (\text{eq. 9})
\]

\[
1.85 \frac{\text{A}}{\mu \text{s}} = \frac{12 \text{ V} - 3.3 \text{ V}}{4.7 \mu \text{H}}
\]

\[L_{\text{OUT}} = \text{Output inductance}
\]

\[V_{\text{IN}} = \text{Input voltage}
\]

\[V_{\text{OUT}} = \text{Output voltage}
\]

Equation 9 implies that larger inductor values limit the regulator’s ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply the load current until the inductor current reaches the output load current level. Reduced inductance to increase slew rates results in larger values of output capacitance to maintain tight output voltage regulation. In contrast, smaller values of inductance increase the regulator’s maximum achievable slew rate and decrease the necessary capacitance at the expense of higher ripple current. The peak-to-peak ripple current for NCP3170 is given by the following equation:

\[
I_{\text{pp}} = \frac{V_{\text{OUT}} \times (1 - D)}{L_{\text{OUT}} \times F_{\text{SW}}} \quad (\text{eq. 10})
\]

\[
1.02 \text{ A} = \frac{3.3 \text{ V} \times (1 - 27.5\%)}{4.7 \mu \text{H} \times 500 \text{ kHz}}
\]

\[D = \text{Duty ratio}
\]

\[F_{\text{SW}} = \text{Switching frequency}
\]

\[I_{\text{pp}} = \text{Peak-to-peak current of the inductor}
\]

\[L_{\text{OUT}} = \text{Output inductance}
\]

\[V_{\text{OUT}} = \text{Output voltage}
\]

From Equation 10, it is clear that the ripple current increases as \(L_{\text{OUT}}\) decreases, emphasizing the trade-off between dynamic response and ripple current.

The power dissipation of an inductor falls into two categories: copper and core losses. Copper losses can be further categorized into DC losses and AC losses. A good first order approximation of the inductor losses can be made using the DC resistance as shown below:

\[
L_{\text{PCU,DC}} = I_{\text{RMS}}^2 \times DCR \rightarrow \quad (\text{eq. 11})
\]

\[
61 \text{ mW} = 3.01^2 \times 6.73 \text{ mΩ}
\]

\[\text{DCR} = \text{Inductor DC resistance}
\]

\[I_{\text{RMS}} = \text{Inductor RMS current}
\]

\[L_{\text{PCU,DC}} = \text{Inductor DC power dissipation}
\]

The core losses and AC copper losses will depend on the geometry of the selected core, core material, and wire used. Most vendors will provide the appropriate information to make accurate calculations of the power dissipation at which point the total inductor losses can be captured by the equation below:

\[
L_{\text{Ptot}} = L_{\text{PCU,DC}} + L_{\text{PCU,AC}} + L_{\text{PCore}} \rightarrow \quad (\text{eq. 12})
\]

\[
67 \text{ mW} = 61 \text{ mW} + 5 \text{ mW} + 1 \text{ mW}
\]

\[L_{\text{PCore}} = \text{Inductor core power dissipation}
\]

\[L_{\text{PCU,AC}} = \text{Inductor AC power dissipation}
\]

\[L_{\text{PCU,DC}} = \text{Inductor DC power dissipation}
\]

\[L_{\text{Ptot}} = \text{Total inductor losses}
\]

**Output Capacitor Selection**

The important factors to consider when selecting an output capacitor are DC voltage rating, ripple current rating, output ripple voltage requirements, and transient response requirements.

The output capacitor must be able to operate properly for the life time of a product. When selecting a capacitor it is important to select a voltage rating that is de-rated to the guaranteed operating life time of a product. Further, it is important to note that when using ceramic capacitors, the capacitance decreases as the voltage applied increases; thus a ceramic capacitor rated at 100 μF 6.3 V may measure 100 μF at 0 V but measure 20 μF with an applied voltage of 3.3 V depending on the type of capacitor selected.

The output capacitor must be rated to handle the ripple current at full load with proper derating. The capacitor RMS ratings given in datasheets are generally for lower switching frequencies than used in switch mode power supplies, but a multiplier is given for higher frequency operation. The RMS current for the output capacitor can be calculated below:

\[
C_{\text{RMS}} = \frac{I_{\text{OUT}} \times ra}{\sqrt{12}} \rightarrow \quad (\text{eq. 13})
\]

\[
0.294 \text{ A} = 3.0 \text{ A} \times 34\% \times \frac{1}{\sqrt{12}}
\]

\[C_{\text{RMS}} = \text{Output capacitor RMS current}
\]

\[I_{\text{OUT}} = \text{Output current}
\]

\[ra = \text{Ripple current ratio}
\]

The maximum allowable output voltage ripple is a combination of the ripple current selected, the output capacitance selected, the Equivalent Series Inductance (ESL), and Equivalent Series Resistance (ESR).

http://onsemi.com

15
The main component of the ripple voltage is usually due to the ESR of the output capacitor and the capacitance selected, which can be calculated as shown in Equation 14:

\[ V_{ESR_C} = I_{OUT} \times ra \times \left( \frac{1}{8 \times F_{SW} \times C_{OUT}} \right) \]

10.89 mV = 3 × 34% × \left( \frac{5 \text{ mΩ} + \frac{1}{8 \times 500 \text{ kHz} \times 44 \text{ μF}}}{} \right) \quad \text{(eq. 14)}

\[ \begin{align*}
C_{ESR} & = \text{Output capacitor ESR} \\
C_{OUT} & = \text{Output capacitance} \\
F_{SW} & = \text{Switching frequency} \\
I_{OUT} & = \text{Output current} \\
ra & = \text{Ripple current ratio} \\
V_{ESR_C} & = \text{Ripple voltage from the capacitor}
\end{align*} \]

The impedance of a capacitor is a function of the frequency of operation. When using ceramic capacitors, the ESR of the capacitor decreases until the resonant frequency is reached, at which point the ESR increases; therefore the ripple voltage might not be what one expected due to the switching frequency. Further, the method of layout can add resistance in series with the capacitance, increasing ripple voltage.

The ESL of capacitors depends on the technology chosen, but tends to range from 1 nH to 20 nH, where ceramic capacitors have the lowest inductance and electrolytic capacitors have the highest. The calculated contributing voltage ripple from ESL is shown for the switch on and switch off below:

\[ V_{ESLON} = \frac{\text{ESL} \times I_{pp} \times F_{SW}}{D} \rightarrow \quad \text{(eq. 15)} \]

1.84 mV = \frac{1 \text{ nH} \times 1.01 \text{ A} \times 500 \text{ kHz}}{27.5\%} \quad \text{(eq. 15)}

\[ \begin{align*}
V_{ESLOFF} & = \frac{\text{ESL} \times I_{pp} \times F_{SW}}{(1 - D)} \rightarrow \\
0.7 \text{ mV} & = \frac{1 \text{ nH} \times 1.1 \text{ A} \times 500 \text{ kHz}}{(1 - 27.5\%)} \quad \text{(eq. 16)}
\end{align*} \]

\[ \begin{align*}
D & = \text{Duty ratio} \\
\text{ESL} & = \text{Capacitor inductance} \\
F_{SW} & = \text{Switching frequency} \\
I_{pp} & = \text{Peak-to-peak current}
\end{align*} \]

The output capacitor is a basic component for fast response of the power supply. For the first few microseconds of a load transient, the output capacitor supplies current to the load. Once the regulator recognizes a load transient, it adjusts the duty ratio, but the current slope is limited by the inductor value.

During a load step transient, the output voltage initially drops due to the current variation inside the capacitor and the ESR (neglecting the effect of the ESL).

\[ \Delta V_{OUT-ESR} = I_{TRAN} \times C_{ESR} \rightarrow \quad \text{(eq. 17)} \]

\[ 7.5 \text{ mV} = 1.5 \text{ A} \times 5 \text{ mΩ} \quad \text{(eq. 17)} \]

\[ \begin{align*}
C_{ESR} & = \text{Output capacitor Equivalent Series Resistance} \\
I_{TRAN} & = \text{Output transient current} \\
\Delta V_{OUT-ESR} & = \text{Voltage deviation of } V_{OUT} \text{ due to the effects of ESR}
\end{align*} \]

A minimum capacitor value is required to sustain the current during the load transient without discharging it. The voltage drop due to output capacitor discharge is given by the following equation:

\[ \Delta V_{OUT-DIS} = \frac{(I_{TRAN})^2 \times L_{OUT} \times F_{SW}}{2 \times F_{CROSS} \times C_{OUT} \times (V_{IN} - V_{OUT})} \rightarrow \quad \text{(eq. 18)} \]

133.5 mV = \frac{(1.5)^2 \times 4.7 \text{ μH} \times 500 \text{ kHz}}{2 \times 50 \text{ kHz} \times 44 \text{ μF} \times (12 \text{ V} - 3.3 \text{ V})} \quad \text{(eq. 18)}

\[ \begin{align*}
C_{OUT} & = \text{Output capacitance} \\
D & = \text{Duty ratio} \\
F_{SW} & = \text{Switching frequency} \\
F_{CROSS} & = \text{Loop cross over frequency} \\
I_{TRAN} & = \text{Output transient current} \\
L_{OUT} & = \text{Output inductor value} \\
V_{IN} & = \text{Input voltage} \\
V_{OUT} & = \text{Output voltage} \\
\Delta V_{OUT-DIS} & = \text{Voltage deviation of } V_{OUT} \text{ due to the effects of capacitor discharge}
\end{align*} \]

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. Please note that \( \Delta V_{OUT-DIS} \) and \( \Delta V_{OUT-ESR} \) are out of phase with each other, and the larger of these two voltages will determine the maximum deviation of the output voltage (neglecting the effect of the ESL). It is important to note that the converters frequency response will change when the NCP3170 is operating in synchronous mode or non–synchronous mode due to the change in plant response from CCM to DCM. The effect will be a larger transient voltage excursion when transitioning from no load to full load quickly.

**Input Capacitor Selection**

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize losses and input voltage ripple. The RMS value of the input ripple current is:

\[ I_{inRMS} = I_{OUT} \times \sqrt{D \times (1 - D)} \rightarrow \quad \text{(eq. 19)} \]

\[ 1.34 \text{ A} = 3 \text{ A} \times \sqrt{27.5\% \times (1 - 27.5\%)} \quad \text{(eq. 19)} \]

\[ \begin{align*}
D & = \text{Duty ratio} \\
I_{inRMS} & = \text{Input capacitance RMS current} \\
I_{OUT} & = \text{Load current}
\end{align*} \]

The equation reaches its maximum value with \( D = 0.5 \) at which point the input capacitance RMS current is half the
output current. Loss in the input capacitors can be calculated with the following equation:

\[ P_{\text{CIN}} = C_{\text{IN}_{\text{ESR}}} \times (I_{\text{inRMS}})^2 \]  
(eq. 20)

\[ 18 \text{ mW} = 10 \text{ m\Omega} \times (1.34 \text{ A})^2 \]

\[ C_{\text{IN}_{\text{ESR}}} = \text{Input capacitance Equivalent Series Resistance} \]

\[ I_{\text{inRMS}} = \text{Input capacitance RMS current} \]

\[ P_{\text{CIN}} = \text{Power loss in the input capacitor} \]

Due to large di/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum capacitor must be used, it must be surge protected, otherwise capacitor failure could occur.

**Power MOSFET Dissipation**

Power dissipation, package size, and the thermal environment drive power supply design. Once the dissipation is known, the thermal impedance can be calculated to prevent the specified maximum junction temperatures from being exceeded at the highest ambient temperature.

Power dissipation has two primary contributors: conduction losses and switching losses. The high−side MOSFET will display both switching and conduction losses. The switching losses of the low side MOSFET will not be calculated as it switches into nearly zero voltage and the losses are insignificant. However, the body diode in the low−side MOSFET will suffer diode losses during the non−overlap time of the gate drivers.

Starting with the high−side MOSFET, the power dissipation can be approximated from:

\[ P_{\text{D,HS}} = P_{\text{COND}} + P_{\text{SW,TOT}} \]  
(eq. 21)

\[ P_{\text{COND}} = \text{Conduction losses} \]

\[ P_{\text{D,HS}} = \text{Power losses in the high side MOSFET} \]

\[ P_{\text{SW,TOT}} = \text{Total switching losses} \]

The first term in Equation 21 is the conduction loss of the high−side MOSFET while it is on.

\[ P_{\text{COND}} = \left(I_{\text{RMS,HS}}\right)^2 \times R_{\text{DS(on),HS}} \]  
(eq. 22)

\[ I_{\text{RMS,HS}} = \text{RMS current in the high side MOSFET} \]

\[ R_{\text{DS(on),HS}} = \text{On resistance of the high side MOSFET} \]

\[ P_{\text{COND}} = \text{Conduction power losses} \]

Using the ra term from Equation 5, IRMS becomes:

\[ I_{\text{RMS,HS}} = I_{\text{OUT}} \times \sqrt{D \times \left(1 + \frac{\text{ra}^2}{12}\right)} \]  
(eq. 23)

\[ D = \text{Duty ratio} \]

\[ \text{ra} = \text{Ripple current ratio} \]

\[ I_{\text{OUT}} = \text{Output current} \]

\[ I_{\text{RMS,HS}} = \text{High side MOSFET RMS current} \]

The second term from Equation 21 is the total switching loss and can be approximated from the following equations.

\[ P_{\text{SW,TOT}} = P_{\text{SW}} + P_{\text{DS}} + P_{\text{RR}} \]  
(eq. 24)

\[ P_{\text{DS}} = \text{High side MOSFET drain to source losses} \]

\[ P_{\text{RR}} = \text{High side MOSFET reverse recovery losses} \]

\[ P_{\text{SW}} = \text{High side MOSFET switching losses} \]

\[ P_{\text{SW,TOT}} = \text{High side MOSFET total switching losses} \]

The first term for total switching losses from Equation 24 are the losses associated with turning the high−side MOSFET on and off and the corresponding overlap in drain voltage and current.

\[ P_{\text{SW}} = P_{\text{TON}} + P_{\text{TOFF}} = \frac{1}{2} \times (I_{\text{OUT}} \times V_{\text{IN}} \times F_{\text{SW}}) \times \left(t_{\text{RISE}} + t_{\text{FALL}}\right) \]  
(eq. 25)

\[ F_{\text{SW}} = \text{Switching frequency} \]

\[ I_{\text{OUT}} = \text{Load current} \]

\[ P_{\text{SW}} = \text{High side MOSFET switching losses} \]

\[ P_{\text{TON}} = \text{Turn on power losses} \]

\[ P_{\text{TOFF}} = \text{Turn off power losses} \]

\[ t_{\text{RISE}} = \text{MOSFET rise time} \]

\[ t_{\text{FALL}} = \text{MOSFET fall time} \]

\[ V_{\text{IN}} = \text{Input voltage} \]

When calculating the rise time and fall time of the high side MOSFET, it is important to know the charge characteristic shown in Figure 44.

![Figure 44. High Side MOSFET Total Charge](http://onsemi.com)

\[ t_{\text{RISE}} = \frac{Q_{\text{GD}}}{I_{G1}} = \frac{Q_{\text{GD}}}{(V_{\text{CL}} - V_{\text{TH}})/(R_{\text{HSPU}} + R_{\text{G}})} \]  
(eq. 26)

\[ I_{G1} = \text{Output current from the high−side gate drive} \]

\[ Q_{\text{GD}} = \text{MOSFET gate drain gate charge} \]

\[ R_{\text{HSPU}} = \text{Drive pull up resistance} \]

\[ R_{\text{G}} = \text{MOSFET gate resistance} \]

\[ V_{\text{CL}} = \text{Clamp voltage} \]

\[ V_{\text{TH}} = \text{MOSFET gate threshold voltage} \]
\[ I_{\text{FALL}} = \frac{Q_{\text{GD}}}{I_{\text{G2}}} = \frac{Q_{\text{GD}}}{(V_{\text{CL}} - V_{\text{TH}})/(R_{\text{HSPD}} + R_{\text{G}})} \]  

(eq. 27)

**IG2** = Output current from the low−side gate drive  
**Q_{\text{GD}}** = MOSFET gate to drain gate charge  
**R_{\text{G}}** = MOSFET gate resistance  
**R_{\text{HSPD}}** = Drive pull down resistance  
**V_{\text{CL}}** = Clamp voltage  
**V_{\text{TH}}** = MOSFET gate threshold voltage

Next, the MOSFET output capacitance losses are caused by both the high−side and low−side MOSFETs, but are dissipated only in the high−side MOSFET.

\[ P_{\text{DS}} = \frac{1}{2} \times C_{\text{OSS}} \times V_{\text{IN}}^2 \times F_{\text{SW}} \]  

(eq. 28)

**C_{\text{OSS}}** = MOSFET output capacitance at 0 V  
**F_{\text{SW}}** = Switching frequency  
**P_{\text{DS}}** = MOSFET drain to source charge losses  
**V_{\text{IN}}** = Input voltage

Finally, the loss due to the reverse recovery time of the body diode in the low−side MOSFET is shown as follows:

\[ P_{\text{RR}} = Q_{\text{RR}} \times V_{\text{IN}} \times F_{\text{SW}} \]  

(eq. 29)

**F_{\text{SW}}** = Switching frequency  
**P_{\text{RR}}** = High side MOSFET reverse recovery losses  
**Q_{\text{RR}}** = Reverse recovery charge  
**V_{\text{IN}}** = Input voltage

The low−side MOSFET turns on into small negative voltages so switching losses are negligible. The low−side MOSFET’s power dissipation only consists of conduction loss due to \( R_{\text{DS(on)}} \) and body diode loss during non−overlap periods.

\[ P_{\text{D,LS}} = P_{\text{COND}} + P_{\text{BODY}} \]  

(eq. 30)

**P_{\text{BODY}}** = Low side MOSFET body diode losses  
**P_{\text{COND}}** = Low side MOSFET conduction losses  
**P_{\text{D,LS}}** = Low side MOSFET losses

Conduction loss in the low−side MOSFET is described as follows:

\[ P_{\text{COND}} = \left( I_{\text{RMS_Ls}} \right)^2 \times R_{\text{DS(on),LS}} \]  

(eq. 31)

**I_{\text{RMS_Ls}}** = RMS current in the low side  
**R_{\text{DS(on),LS}}** = Low−side MOSFET on resistance  
**P_{\text{COND}}** = High side MOSFET conduction losses

\[ I_{\text{RMS_Ls}} = I_{\text{OUT}} \times \sqrt{\left(1 - D\right) \times \left(1 + \frac{ra^2}{12}\right)} \]  

(eq. 32)

**D** = Duty ratio  
**I_{\text{OUT}}** = Load current  
**I_{\text{RMS_Ls}}** = RMS current in the low side  
**ra** = Ripple current ratio

The body diode losses can be approximated as:

\[ P_{\text{BODY}} = V_{\text{FD}} \times I_{\text{OUT}} \times F_{\text{SW}} \times (NOL\text{LH} + NOL\text{HH}) \]  

(eq. 33)

**F_{\text{SW}}** = Switching frequency  
**I_{\text{OUT}}** = Load current  
**NOL\text{LH}** = Dead time between the high−side MOSFET turning off and the low−side MOSFET turning on, typically 30 ns  
**NOLLH** = Dead time between the low−side MOSFET turning off and the high−side MOSFET turning on, typically 30 ns  
**P_{\text{BODY}}** = Low−side MOSFET body diode losses  
**V_{\text{FD}}** = Body diode forward voltage drop typically 0.92 V

**Compensation Network**

To create a stable power supply, the compensation network around the transconductance amplifier must be used in conjunction with the PWM generator and the power stage. Since the power stage design criteria is set by the application, the compensation network must correct the overall output to ensure stability. The NCP3170 is a current mode regulator and as such there exists a voltage loop and a current loop. The current loop causes the inductor to act like a current source which governs most of the characteristics of current mode control. The output inductor and capacitor of the power stage form a double pole but because the inductor is treated like a current source in closed loop, it becomes a single pole system. Since the feedback loop is controlling the inductor current, it is effectively like having a current source feeding a capacitor; therefore the pole is controlled by the load and the output capacitance. A table of compensation values for 500 kHz and 1 MHz is provided below for two 22 μF ceramic capacitors. The table also provides the resistor value for CompCalc at the defined operating point.
<table>
<thead>
<tr>
<th>VIN  (V)</th>
<th>Vout (V)</th>
<th>Lout (μF)</th>
<th>R1  (kΩ)</th>
<th>R2  (kΩ)</th>
<th>RF  (kΩ)</th>
<th>CF  (pF)</th>
<th>CC  (nF)</th>
<th>RC  (kΩ)</th>
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<td>82</td>
<td>1.8</td>
<td>10</td>
<td>NI</td>
<td></td>
</tr>
</tbody>
</table>
To compensate the converter we must first calculate the current feedback

\[
M = \frac{32 \times \frac{V_{\text{out}}}{V_{\text{in}}} + 1.46}{V_{\text{Vin}}} \times F_{\text{SW}} \times L_{\text{OUT}} \quad \text{(eq. 34)}
\]

\(F_{\text{SW}}\) = Switching Frequency  
\(L_{\text{OUT}}\) = Output inductor value  
\(M\) = Current feedback  
\(V_{\text{in}}\) = Input Voltage  
\(V_{\text{OUT}}\) = Output Voltage

The un-scaled gain of the converter also needs to be calculated as follows:

\[
A = \frac{1}{\frac{I_{\text{OUT}}}{V_{\text{O}}} - M \times 0.5 \times \frac{V_{\text{out}}}{V_{\text{Vin}}} \times \frac{V_{\text{out}}}{V_{\text{Vin}}} \times \frac{L_{\text{OUT}}}{L_{\text{OUT}} \times F_{\text{SW}}}}
\]

\(0.339 \, \Omega\) \quad \text{(eq. 35)}

\(A\) = Un-scaled gain  
\(F_{\text{SW}}\) = Switching Frequency  
\(I_{\text{OUT}}\) = Output Current  
\(L_{\text{OUT}}\) = Output inductor value  
\(M\) = Current feedback  
\(V_{\text{IN}}\) = Input Voltage  
\(V_{\text{OUT}}\) = Output Voltage

Next the DC gain of the plant must be calculated.

\[
G = \frac{A}{32 \times \frac{V_{\text{out}}}{V_{\text{Vin}}} + 1.46} \quad \text{(eq. 36)}
\]

\(33.061 = \frac{A}{32 \times \frac{3.3 \, \text{V}}{12 \, \text{V}} + 1.46} \, \text{m}\Omega\)

\(F_{\text{SW}}\) = Switching Frequency  
\(G\) = DC gain of the plant  
\(L_{\text{OUT}}\) = Output inductor value  
\(I_{\text{OUT}}\) = Output current  
\(M\) = Current feedback  
\(V_{\text{IN}}\) = Input voltage  
\(V_{\text{OUT}}\) = Output voltage

The amplitude ratio can be calculated using the following equation:

\[
Y = \frac{V_{\text{REF}}}{V_{\text{OUT}}} \rightarrow 0.242 = \frac{0.8 \, \text{V}}{3.3 \, \text{V}} \quad \text{(eq. 37)}
\]

\(V_{\text{O}}\) = Output voltage  
\(V_{\text{REF}}\) = Regulator reference voltage  
\(Y\) = Amplitude ratio

The ESR of the output capacitor creates a “zero” at the frequency as shown in Equation 38:

\[
F_{\text{ZESR}} = \frac{1}{2\pi \times C_{\text{OESR}} \times C_{\text{OUT}}} \rightarrow
\]

\(723 \, \text{kHz} = \frac{1}{2\pi \times 0.005 \, \text{m}\Omega \times 44 \, \mu\text{F}} \quad \text{(eq. 38)}

\(C_{\text{OESR}}\) = Output capacitor ESR  
\(C_{\text{OUT}}\) = Output capacitor  
\(F_{\text{ZESR}}\) = Output capacitor zero ESR frequency

\[
F_{\text{P}} = \frac{1}{2\pi \times A \times C_{\text{OUT}}} \rightarrow
\]

\(10.664 \, \text{kHz} = \frac{1}{2\pi \times 0.339 \, \Omega \times 44 \, \mu\text{F}} \quad \text{(eq. 39)}

\(A\) = Un-scaled gain  
\(C_{\text{OUT}}\) = Output capacitor  
\(F_{\text{P}}\) = Current mode pole frequency

The two equations above define the bode plot that the power stage has created or open loop response of the system. The next step is to close the loop by considering the feedback values. The closed loop crossover frequency should be less than 1/10 of the switching frequency, which would place the maximum crossover frequency at 50 kHz.

Figure 45 shows a pseudo Type III transconductance error amplifier.

\[
\text{Figure 45. Pseudo Type III Transconductance Error Amplifier}
\]

The compensation network consists of the internal error amplifier and the impedance networks \(Z_{\text{IN}} (R_1, R_2, \text{and} \, C_F)\) and external \(Z_{\text{FB}} (R_C, C_C, \text{and} \, C_P)\). The compensation network has to provide a closed loop transfer function with
the highest 0 dB crossing frequency to have fast response and the highest gain in DC conditions, so as to minimize load regulation issues. A stable control loop has a gain crossing with −20 dB/decade slope and a phase margin greater than 45°. Include worst-case component variations when determining phase margin. To start the design, a resistor value should be chosen for R1 from which all other components can be chosen. A good starting value is 24.9 kΩ.

The NCP3170 allows the output of the DC–DC regulator to be adjusted down to 0.8 V via an external resistor divider network. The regulator will maintain 0.8 V at the feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to VOUT, the regulator will regulate the output voltage proportional to the resistor divider network in order to maintain 0.8 V at the FB pin.

![Figure 46. Feedback Resistor Divider](image)

The relationship between the resistor divider network above and the output voltage is shown in Equation 40:

\[
R_2 = R_1 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}}\right) \quad \text{(eq. 40)}
\]

- \(R_1\) = Top resistor divider
- \(R_2\) = Bottom resistor divider
- \(V_{OUT}\) = Output voltage
- \(V_{REF}\) = Regulator reference voltage

The most frequently used output voltages and their associated standard \(R_1\) and \(R_2\) values are listed in the table below.

**OUTPUT VOLTAGE SETTINGS**

<table>
<thead>
<tr>
<th>(V_O) (V)</th>
<th>(R_1) (kΩ)</th>
<th>(R_2) (kΩ)</th>
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<tbody>
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</table>

The compensation components for the Pseudo Type III Transconductance Error Amplifier can be calculated using the method described below. The method serves to provide a good starting place for compensation of a power supply. The values can be adjusted in real time using the compensation tool CompCalc [http://www.onsemi.com/pub/Collateral/COMPCALC.ZIP](http://www.onsemi.com/pub/Collateral/COMPCALC.ZIP).

The first pole to crossover at the desired frequency should be setup at \(F_{PO}\) to decrease at −20 dB per decade:

\[
F_{PO} = \frac{F_{CROSS}}{G} \quad \text{(eq. 41)}
\]

\[
1.512 \text{ kHz} = \frac{50 \text{ kHz}}{33.061} \quad \text{1.512 kHz = Cross over frequency}
\]

\[
F_{CROSS} = \text{Cross over frequency}
\]

\[
F_{PO} = \text{Pole frequency to meet crossover frequency}
\]

\[
G = \text{DC gain of the plant}
\]

The crossover combined compensation network can be used to calculate the transconductance output compensation network as follows:

\[
C_C = \frac{y \times g_m}{2 \times \pi \times F_{PO}} \quad \text{(eq. 42)}
\]

\[
5.12 \text{ nF} = \frac{0.242 \times 200 \mu\text{s}}{2\pi \times 1.512 \text{ kHz}}
\]

- \(C_C\) = Compensation capacitor
- \(F_{PO}\) = Pole frequency
- \(g_m\) = Transconductance of amplifier
- \(y\) = Amplitude ratio

\[
R_C = \frac{1}{2\pi \times C_C \times F_P} \quad \text{(eq. 43)}
\]

\[
2.925 \text{ kΩ} = \frac{1}{2\pi \times 5.12 \text{ nF} \times 1.512 \text{ kHz}}
\]

- \(C_C\) = Compensation capacitance
- \(C_{OUT}\) = Output capacitance
- \(F_P\) = Current mode pole frequency
- \(R_C\) = Compensation resistor

\[
C_P = \frac{1}{2\pi \times R_C \times F_{ESR}} \quad \text{(eq. 44)}
\]

\[
75.2 \text{ pF} = \frac{1}{2\pi \times 2.925 \text{ kΩ} \times 723 \text{ kHz}}
\]

- \(C_P\) = Compensation pole capacitor
- \(F_{ESR}\) = Capacitor ESR zero frequency
- \(R_C\) = Compensation resistor

If the ESR frequency is greater than the switching frequency, a CF compensation capacitor may be needed for stability as the output LC filter is considered high Q and thus will not give the phase boost at the crossover frequency. Further at low duty cycles due to some blanking and filtering of the current signal the current gain of the converter is not constant and the current gain is small. Thus adding CF and RF can give the needed phase boost.
Calculating Input Inrush Current

The input inrush current has two distinct stages: input charging and output charging. The input charging of a buck stage is usually controlled, but there are times when it is not and is limited only by the input RC network, and the output impedance of the upstream power stage. If the upstream power stage is a perfect voltage source and switches on instantaneously, then the input inrush current can be depicted as shown in Figure 47 and calculated as:

\[
C_F = \frac{R1 + R2}{2\pi \times (R1 * RF + R2 * RF + R2 * R1)} \times F_{\text{cross}}
\]

127 pF = \frac{24.9 \, k\Omega + 7.87 \, k\Omega}{2\pi \times (24.9 \, k\Omega \times 1 \, k\Omega + 7.87 \, k\Omega \times 1 \, k\Omega + 7.87 \, k\Omega \times 24.9 \, k\Omega)} \times 50 \, kHz

\begin{align*}
C_F &= \text{Compensation pole capacitor} \\
F_{\text{cross}} &= \text{Cross over frequency} \\
gm &= \text{Transconductance of amplifier} \\
R1 &= \text{Top resistor divider} \\
R2 &= \text{Bottom resistor divider} \\
RF &= \text{Feed through resistor}
\end{align*}

\[
F_{\text{cross}} = \frac{24.9 \, k\Omega \times 1 \, k\Omega + 7.87 \, k\Omega \times 1 \, k\Omega + 7.87 \, k\Omega \times 24.9 \, k\Omega}{2\pi \times (R1 * RF + R2 * RF + R2 * R1)} \times 50 \, kHz
\]

From the above equation, it is clear that the inrush current is dependent on the type of load that is connected to the output. Two types of load are considered in Figure 48: a resistive load and a stepped current load.

If the load is resistive in nature, the output current will increase with soft start linearly which can be quantified in Equation 49.

\[
I_{\text{CLR R}_{\text{MS}}} = \frac{1}{\sqrt[3]{3}} \times \frac{V_{\text{OUT}}}{R_{\text{OUT}}} \quad I_{\text{CLR PK}} = \frac{V_{\text{OUT}}}{R_{\text{OUT}}}
\]

191 mA = \frac{1}{\sqrt[3]{3}} \times \frac{3.3 \, V}{10 \, \Omega} \quad \frac{300 \, mA}{10 \, \Omega}

\begin{align*}
I_{\text{CLR R}_{\text{MS}}} &= \text{RMS resistor current} \\
I_{\text{CLR PK}} &= \text{Peak resistor current} \\
R_{\text{OUT}} &= \text{Output resistance} \\
V_{\text{OUT}} &= \text{Output voltage}
\end{align*}

Once the t\text{DELAY TOTAL} has expired, the buck converter starts to switch and a second inrush current can be calculated:

\[
I_{\text{OC inrush RMS}} = \left( \frac{C_{\text{OUT}} + C_{\text{LOAD}}}{t_{\text{SS}}} \times \frac{V_{\text{OUT}} \times D}{\sqrt[3]{3}} \right) + I_{\text{CL}} \times D
\]

\begin{align*}
C_{\text{OUT}} &= \text{Total converter output capacitance} \\
C_{\text{LOAD}} &= \text{Total load capacitance} \\
D &= \text{Duty ratio of the load} \\
I_{\text{CL}} &= \text{Applied load at the output} \\
I_{\text{OC inrush RMS}} &= \text{RMS inrush current during start-up} \\
t_{\text{SS}} &= \text{Soft start interval} \\
V_{\text{OUT}} &= \text{Output voltage}
\end{align*}

Figure 47. Input Charge Inrush Current

\[
I_{\text{IC inrush PK}} = \frac{V_{\text{IN}}}{C_{\text{IN}}} \\
I_{\text{IC inrush RMS}} = \frac{V_{\text{IN}}}{C_{\text{IN}ESR}} + 0.316 \times \sqrt{\frac{5 \times C_{\text{IN}ESR} \times C_{\text{IN}}}{t_{\text{DELAY TOTAL}}}}
\]

12.58 A = 12 V \times 0.316 \times \sqrt{\frac{5 \times 0.01 \, \Omega \times 22 \, pF}{1 \, \text{ms}}}

\[
C_{\text{IN}} = \text{Output capacitor} \\
C_{\text{IN}ESR} = \text{Output capacitor ESR} \\
t_{\text{DELAY TOTAL}} = \text{Total delay interval} \\
V_{\text{IN}} = \text{Input Voltage}
\]

Once the t\text{DELAY TOTAL} has expired, the buck converter starts to switch and a second inrush current can be calculated:

\[
I_{\text{IC inrush RMS}} = \left( \frac{C_{\text{OUT}} + C_{\text{LOAD}}}{t_{\text{SS}}} \times \frac{V_{\text{OUT}} \times D}{\sqrt[3]{3}} \right) + I_{\text{CL}} \times D
\]

\begin{align*}
C_{\text{OUT}} &= \text{Total converter output capacitance} \\
C_{\text{LOAD}} &= \text{Total load capacitance} \\
D &= \text{Duty ratio of the load} \\
I_{\text{CL}} &= \text{Applied load at the output} \\
I_{\text{OC inrush RMS}} &= \text{RMS inrush current during start-up} \\
t_{\text{SS}} &= \text{Soft start interval} \\
V_{\text{OUT}} &= \text{Output voltage}
\end{align*}

Figure 48. Load Connected to the Output Stage

Figure 49. Resistive Load Current

http://onsemi.com
Alternatively, if the output load has an under voltage lockout, turns on at a defined voltage level, and draws a constant current, then the RMS connected load current is:

$$I_{CL1} = \sqrt{\frac{V_{OUT} - V_{OUT\_TO}}{V_{OUT}}} \times I_{OUT}$$  
(eq. 50)

$$492 \text{ mA} = \sqrt{\frac{3.3 \text{ V} - 2.5 \text{ V}}{3.3 \text{ V}}} \times 1 \text{ A}$$

$I_{OUT}$ = Output current  
$V_{OUT}$ = Output voltage  
$V_{OUT\_TO}$ = Output voltage load turn on

**Figure 50. Voltage Enable Load Current**

If the inrush current is higher than the steady state input current during max load, then an input fuse should be rated accordingly using $I^2t$ methodology.

**Thermal Management and Layout**

**Consideration**

In the NCP3170 buck regulator high pulsing current flows through two loops as shown in the figure below.

The first loop shown in blue activates when the high side switch turns on. When the switch turns on, the edge of the current waveform is provided by the bypass capacitor. The remainder of the current is provided by the input capacitor. Slower currents are provided by the upstream power supply which fills up the input capacitor when the high side switch is off. The current flows through the high side MOSFET and to the output, charging the output capacitors and providing current to the load. The current returns through a PCB ground trace where the output capacitors are connected, the regulator is grounded, and the input capacitors are grounded.

The second loop starts from the inductor to the output capacitors and load, and returns through the low side MOSFET. Current flows in the second loop when the low side NMOSFET is on. The designer should note that there are locations where the red line and the blue line overlap; these areas are considered to have DC current. Areas containing a single blue line indicate that AC currents flow and transition very quickly. The key to power supply layout is to focus on the connections where the AC current flows.

A good rule of thumb is that for every inch of PCB trace, 20 nH of inductance exists. When laying out a PCB, minimizing the AC loop area reduces the noise of the circuit and improves efficiency. A ground plane is strongly recommended to connect the input capacitor, output capacitor, and PGND pin of the NCP3170. Drawing the real high power current flow lines on the recommended layout is important so the designer can see where the currents are flowing.
The NCP3170 is the major source of power dissipation in the system for which the equations above detailed the loss mechanisms. The control portion of the IC power dissipation is determined by the formula below:

\[ P_C = I_C \times V_{IN} \quad \text{(eq. 51)} \]

- \( I_C \) = Control circuitry current draw
- \( P_C \) = Control power dissipation
- \( V_{IN} \) = Input voltage

Once the IC power dissipations are determined, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient temperature. The formula for calculating the junction temperature with the package in free air is:

\[ T_J = T_A + P_D \times R_{thJA} \quad \text{(eq. 52)} \]

- \( P_D \) = Power dissipation of the IC
- \( R_{thJA} \) = Thermal resistance junction to ambient of the regulator package
- \( T_A \) = Ambient temperature
- \( T_J \) = Junction temperature

The thermal performance of the NCP3170 is strongly affected by the PCB layout. Extra care should be taken by users during the design process to ensure that the IC will operate under the recommended environmental conditions. As with any power design, proper laboratory testing should be performed to ensure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e., worst case MOSFET \( R_{DS(on)} \)). Several layout tips are listed below for the best electric and thermal performance. Figure 53 illustrates a PCB layout example of the NCP3170.

1. The VSW pin is connected to the internal PFET and NFET drains, which are a low resistance thermal path. Connect a large copper plane to the VSW pin to help thermal dissipation. If the PG pin is not used in the design, it can be connected to the VSW plane, further reducing the thermal impedance. The designer should ensure that the VSW thermal plane is rounded at the corners to reduce noise.

2. The user should not use thermal relief connections to the VIN and the PGND pins. Construct a large plane around the PGND and VIN pins to help thermal dissipation.

3. The input capacitor should be connected to the VIN and PGND pins as close as possible to the IC.

4. A ground plane on the bottom and top layers of the PBC board is preferred. If a ground plane is not used, separate PGND from AGND and connect them only at one point to avoid the PGND pin noise coupling to the AGND pin.

5. Create copper planes as short as possible from the VSW pin to the output inductor, from the output inductor to the output capacitor, and from the load to PGND.

6. Create a copper plane on all of the unused PCB area and connect it to stable DC nodes such as: \( V_{IN} \), GND, or \( V_{OUT} \).

7. Keep sensitive signal traces far away from the VSW pins or shield them.
**PACKAGE DIMENSIONS**

**SOIC−8 NB**  
**CASE 751−07**  
**ISSUE AK**

**NOTES:**
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.*

**SOLDERING FOOTPRINT**

![Soldering Footprint Diagram](image)

**SCALE 6:1**

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